In the Certificate of Correction Branch
Request for Certificate of Correction Under 37 C.F.R. 1.322

Patent Number	**6,996,799 B1**
Issue Date	02/07/2006
Application Number	09/634,131
Filing Date	08/08/2000
First Named Inventor	Cismas
Title	Automatic Code Generation for Integrated Circuit Design
Group Art Unit	**2193**
Examiner Name	**Wood, William H.**
Docket Number	QUA-102

Certificate
FEB 2 4 2006
of Correction

CERTIFICATE OF MAILING/TRANSMISSION			
I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Attn: Certificate of Correction Branch, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date marked below.			
TYPED OR PRINTED NAME:	ANDREI D. POPOVICI		
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Certificate of Correction Branch
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Sir/Madam:

Please correct the above-referenced patent as shown on the enclosed form PTO/SB/44.

The listed error occurred through the fault of the Office, and is clearly disclosed in the records of the Office. Attached is a copy of a page from a claim listing submitted in an Amendment filed on 05/17/2004, showing the correct word --language-- rather than "lance" in claim 1, paragraph (b).

Applicants respectfully request an expedited issuance of a Certificate of Correction of Office Mistake under 37 C.F.R. 1.322 (see MPEP 1480.01).

Respectfully submitted, Date: 2/15/2006

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,996,799 B1

APPLICATION NO.: 09/634,131

ISSUE DATE : Feb. 7, 2006

INVENTOR(S) : Cismas et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 1, line 52: replace "lance" with --language--

MAILING ADDRESS OF SENDER (Please do not use customer number below):
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CLAIMS

The following listing of claims replaces all prior versions or listings of claims pending in the application:

1. (currently amended) A computer-implemented method of designing an integrated circuit, comprising the steps of:
   a) establishing a central specification for the integrated circuit, the central specification designating a plurality of cores and a plurality of interconnections between the cores;
   b) establishing a set of software language models for the cores, each software language model implementing an internal algorithm of one of the cores;
   c) establishing a set of hardware description language models for the cores, each hardware description language model implementing an internal logic of one of the cores;
   d) generating software language core interconnection code for interconnecting the software language models according to the central specification, to generate a software language model of the circuit; and
   e) generating hardware description language core interconnection code for interconnecting the hardware description language models according to the central specification, to generate a hardware description language model of the circuit~~, the hardware description language core interconnection code designating a set of intercore handshake connections and a set of corresponding intercore data connections~~.

2. (original) The method of claim 1 wherein:
   a) the central specification designates a set of input tokens and a set of output tokens for each core; and
   b) the central specification designates a set of token fields for each interconnection.

3. (original) The method of claim 2 wherein generating the hardware description language core interconnection code comprises generating a set of port declarations from the sets of token fields, input tokens, and output tokens defined in the central specification.